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CS 281

Programming Assignment 2

11/30/11

We were tasked (as a group) to create an 8 bit multiplier in VHDL. The multiplier is the 3-rd version we discussed in class, which has a finite state machine and a clock (except we were given an adder to use instead of our alu).

The code submitted with this lab was created in Sonata VHDL on a Windows 7 64-bit machine.

To run the files in this assignment you must have access to a VHDL simulator (i.e. Sonata). Load the appropriate files in the simulator (all .vhd files included with this submission) and add the appropriate level to the top-level (multiplier tester). You can now simulate using the test bench included.

Testing for this assignment was a frustrating a painstaking task for us. It was tough to time when one multiplication process would be done and when another would begin (so we could do a reset on the HILO registers). Our code works perfectly except for one flaw: when the least significant bit is 1 and the mcand should be added to the HI register, our code shifts first and then adds. We worked for an extremely long time attempting to overcome this problem but could not. This is the only reason our output values are just a little off.